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Inventor(s): C.W. Jones

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Title: METHOD AND APPARATUS FOR GENERATING AN OPTIMAL TEST PATTERN FOR SEQUENCE DETECTION

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U.S. Patent Documents

Examiner Initial	No.	Patent No.	Date	Patentee	Class	Sub-class	Filing Date
/JPT/	A	5383143	01/1995	Crouch et al.			
/JPT/	B	5144230	09/1992	Katoozi et al.			
/JPT/	C	5258986	11/1993	Zerbe			
/JPT/	D	5390192	02/1995	Fujieda			
/JPT/	E	5568437	10/1996	Jamal			
/JPT/	F	5541942	07/1996	Strouss			

Foreign Patent or Published Foreign Patent Application

Examiner Initial	No.	Document No.	Publication Date	Country or Patent Office	Class	Sub-class	Translation
	G						Yes No

Other Documents

Examiner Initial	No.	Author, Title, Date, Place (e.g. Journal) of Publication
/JPT/	H	Mississippi State University; EE3111 DIGITAL DEVICES DESIGN LABORATORY MANUAL, Fourth Edition; Jan. 1994
/JPT/	I	Manoj Franklin and Kewal K. Saluja; EMBEDDED RAM TESTING; 1995 IEEE; pp.29-33
/JPT/	J	H. Maeno, K. Nii, S. Sakayanagi and S. Kato; "LSSD COMPATIBLE AND CONCURRENTLY TESTABLE RAM;" 1992 International Test Conference Proceedings, IEEE; pp. 608-614
/JPT/	K	H. Maeno, T. Hanibuchi, T. Tada, R. Walters, and T. Eto, "TESTING OF EMBEDDED RAM USING EXHAUSTIVE RANDOM SEQUENCES;" 1987 International Test Conference, IEEE; pp. 105-110
Examiner /John P Trimmings/		Date Considered 05/10/2010

Examiner: Initial citation considered. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.